

MITSUBISHI LSIs

M5M29FB/T800FP, VP, RV-80, -10, -12

8,388,608-BIT (1048,576-WORD BY 8-BIT / 524,288-WORD BY16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

DESCRIPTION

The MITSUBISHI M5M29FB/T800FP, VP, RV are 3.3V-only high speed 8,388,608-bit CMOS boot block Flash Memories suitable for mobile and personal computing, and communication products. The M5M29FB/T800FP, VP, RV are fabricated by CMOS technology for the peripheral circuits and DINOR(Divided bit line NOR) architecture for the memory cells, and are available in 44pin SOP or 48pin TSOP(I).

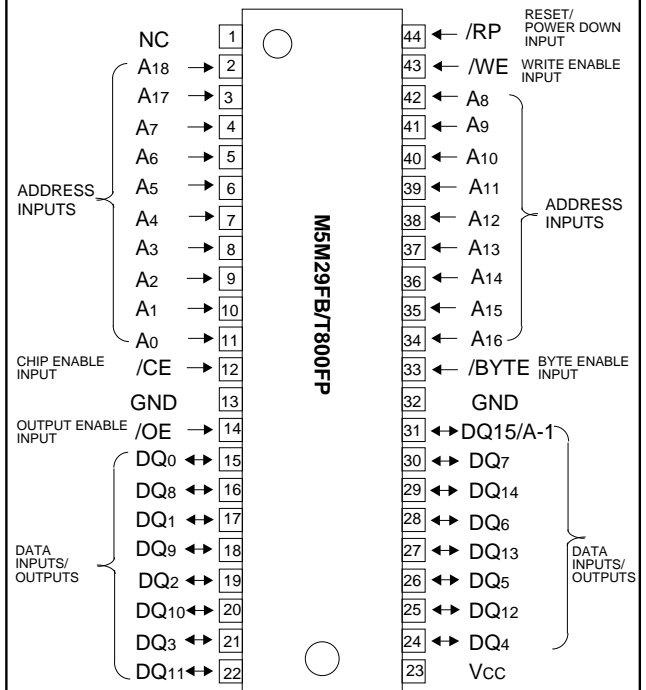
FEATURES

- Organization
 - 524,288 word x 16bit
 - 1,048,576 word x 8 bit
- Supply voltage Vcc = 3.3V±0.3V
- Access time 80/100/120ns (Max)
- Power Dissipation
 - Read 108 mW (Max.)
 - Program/Erase 144 mW (Max.)
 - Standby 0.72 mW (Max.)
 - Deep power down mode 3.3µW (typ.)
- Auto program
 - Program Time 7.5ms (typ.)
 - Program Unit 128word
- Auto Erase
 - Erase time 50 ms (typ.)
 - Erase Unit
 - Boot Block 8Kword / 16Kbyte x 1
 - Parameter Block 4Kword / 8Kbyte x 2
 - Main Block 16Kword / 32Kbyte x 1
 - 32Kword / 64Kbyte x 15
- Program/Erase cycles 100Kcycles
- Boot Block
 - M5M29FB800 Bottom Boot
 - M5M29FT800 Top Boot
- Other Functions
 - Software Command Control
 - Selective Block Lock
 - Erase Suspend/Resume
 - Program Suspend/Resume
 - Status Register Read
 - Sleep
- Package
 - 48-Lead, 12mmx 20mm TSOP (type-I)
 - 44-Lead SOP

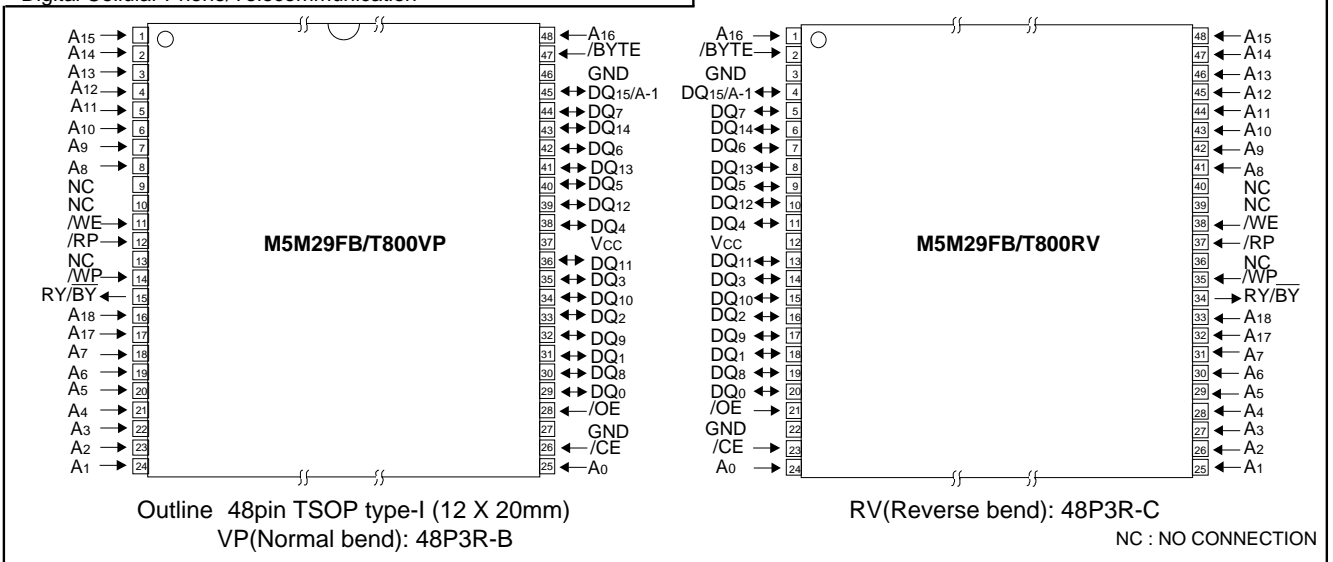
APPLICATION

Code Storage PC BIOS
Digital Cellular Phone/Telecommunication

PIN CONFIGURATION (TOP VIEW)



Outline 600mil 44-pin SOP
(FP: 44P2A-A)



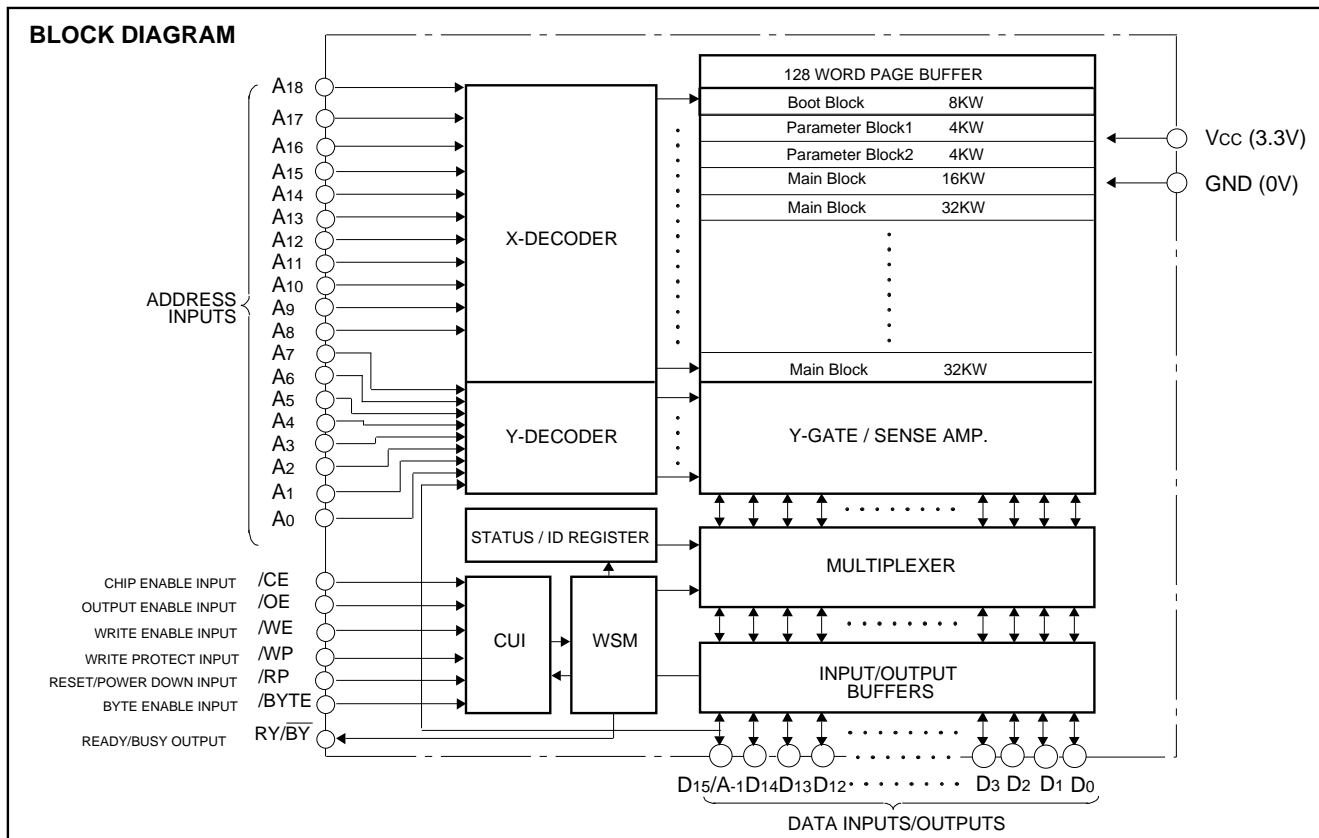
Outline 48pin TSOP type-I (12 X 20mm)
VP(Normal bend): 48P3R-B

RV(Reverse bend): 48P3R-C
NC : NO CONNECTION

This product is compatible with HN29WB/T800 by Hitachi Ltd.

M5M29FB/T800FP,VP,RV-80,-10,-12

8,388,608-BIT (1048,576-WORD BY 8-BIT / 524,288-WORD BY16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY



FUNCTION

The M5M29FB/T800FP,VP,RV includes on-chip program/erase control circuitry. The Write State Machine (WSM) controls block erase and page program operations. Operational modes are selected by the commands written to the Command User Interface (CUI). The Status Register indicates the status of the WSM and when the WSM successfully completes the desired program or block erase operation. A Deep Powerdown mode is enabled when the /RP pin is at GND, minimizing power consumption.

Read

The M5M29FB/T800FP,VP,RV has three read modes, which accesses to the memory array, the Device Identifier and the Status Register. The appropriate read command are required to be written to the CUI. Upon initial device powerup or after exit from deep powerdown, the M5M29FB/T800 automatically resets to read array mode. In the read array mode, low level input to /CE and /OE, high level input to /WE and /RP, and address signals to the address inputs (A0-A18) output the data of the addressed location to the data input/output(D0-15).

Write

Writes to the CUI enables reading of memory array data, device identifiers and reading and clearing of the Status Register. They also enable block erase and program. The CUI is written by bringing /WE to low level, while /CE is at low level and /OE is at high level. Address and data are latched on the earlier rising edge of /WE and /CE. Standard micro-processor write timings are used.

Output Disable

When /OE is at VIH, output from the devices is disabled. Data input/output are in a high-impedance(High-Z) state.

Standby

When /CE is at VIH, the device is in the standby mode and its power consumption is reduced. Data input/output are in a high-impedance(High-Z) state. If the memory is deselected during block erase or program, the internal control circuits remain active and the device consume normal active power until the operation completes.

Deep Power-Down

When /RP is at VIL, the device is in the deep powerdown mode and its power consumption is substantially low. During read modes, the memory is deselected and the data input/output are in a high-impedance(High-Z) state. After return from powerdown, the CUI is reset to Read Array, and the Status Register is cleared to value 80H. During block erase or program modes, /RP low will abort either operation. Memory array data of the block being altered become invalid.

M5M29FB/T800FP, VP, RV-80, -10, -12

8,388,608-BIT (1048,576-WORD BY 8-BIT / 524,288-WORD BY16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

SOFTWARE COMMAND DEFINITIONS

The device operations are selected by writing specific software command into the Command User Interface.

Read Array Command (FFH)

The device is in Read Array mode on initial device powerup and after exit from deep powerdown, or by writing FFH to the Command User Interface. The device remains in Read Array mode until the other commands are written.

Read Device Identifier Command (90H)

Though PROM programmers can normally read device identifier codes by raising A9 to V_{DD}, multiplexing high voltage onto address lines is not desired for micro-processor system. It is an other means to read device identifier codes that Read Device Identifier Code Command(90H) is written to the command latch. Following the command write, the manufacturer code and the device code can be read from address 0000H and 0001H, respectively.

Read Status Register Command (70H)

The Status Register is read after writing the Read Status Register command of 70H to the Command User Interface.

The contents of Status Register are latched on the later falling edge of /OE or /CE. So /CE or /OE must be toggled every status read.

Clear Status Register Command (50H)

The Erase Status and Program Status bits are set to "1"s by the Write State Machine and can only be reset by the Clear Status Register command of 50H. These bits indicates various failure conditions.

Block Erase / Confirm Command (20H/D0H)

Automated block erase is initiated by writing the Block Erase command of 20H followed by the Confirm command of D0H. An address within the block to be erased is required. The WSM executes iterative erase pulse application and erase verify operation.

Page Program Commands(41H)

Page Program allows fast programming of 128words of data. Writing of 41H initiates the page program operation. From 2nd cycle to 129th cycle write data must be serially inputted. Address A6-0 have to be incremented from 00H to 7FH. After completion of data loading, the WSM controls the program pulse application and verify operation.

Basically re-program must not be done on a page which has already programmed.

Suspend/Resume Command (B0H/D0H)

Writing the Suspend command of B0H during block erase operation interrupts the block erase operation and allows read out from another block of memory. Writing the Suspend command of B0H during program operation interrupts the program operation and allows read out from another block of memory. The device continues to output Status Register data when read, after the Suspend command is written to it. Polling the WSM Status and Suspend Status bits will determine when the erase operation or program operation has been suspended. At this point, writing of the Read Array command to the CUI enables reading data from blocks other than that which is suspended. When the Resume command of D0H is written to the CUI, the WSM will continue with the erase or program processes.

DATA PROTECTION

The M5M29FB/T800 provides selectable block locking of memory blocks. Each block has an associated nonvolatile lock-bit which determines the lock status of the block. In addition, the M5M29FB/T800 has a master Write Protect pin (WP) which prevents any modifications to memory blocks whose lock-bits are set to "0", when /WP is low. When /WP is high or /RP is V_{HH}, all blocks can be programmed or erased regardless of the state of the lock-bits, and the lock-bits are cleared to "1" by erase.

Power Supply Voltage

When the power supply voltage (V_{cc}) is less than 2.2V, the device is set to the Read-only mode.

A delay time of 2 us is required before any device operation is initiated. The delay time is measured from the time V_{cc} reaches V_{ccmin} (3.0V).

During power up, /RP=GND is recommended. Falling in Busy status is not recommended for possibility of damaging the device.

M5M29FB/T800FP, VP, RV-80, -10, -12

8,388,608-BIT (1048,576-WORD BY 8-BIT / 524,288-WORD BY16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

x8 (Byte mode) x16 (Word mode)		
F0000H-FFFFFH	78000H-7FFFFH	32Kword MAIN BLOCK
E0000H-EFFFFH	70000H-77FFFH	32Kword MAIN BLOCK
D0000H-DFFFFH	68000H-6FFFFH	32Kword MAIN BLOCK
C0000H-CFFFFH	60000H-67FFFH	32Kword MAIN BLOCK
B0000H-BFFFFH	58000H-5FFFFH	32Kword MAIN BLOCK
A0000H-AFFFFH	50000H-57FFFH	32Kword MAIN BLOCK
90000H-9FFFFH	48000H-4FFFFH	32Kword MAIN BLOCK
80000H-8FFFFH	40000H-47FFFH	32Kword MAIN BLOCK
70000H-7FFFFH	38000H-3FFFFH	32Kword MAIN BLOCK
60000H-6FFFFH	30000H-37FFFH	32Kword MAIN BLOCK
50000H-5FFFFH	28000H-2FFFFH	32Kword MAIN BLOCK
40000H-4FFFFH	20000H-27FFFH	32Kword MAIN BLOCK
30000H-3FFFFH	18000H-1FFFFH	32Kword MAIN BLOCK
20000H-2FFFFH	10000H-17FFFH	32Kword MAIN BLOCK
10000H-1FFFFH	08000H-0FFFFH	32Kword MAIN BLOCK
08000H-0FFFFH	04000H-07FFFH	16Kword MAIN BLOCK
06000H-07FFFH	03000H-03FFFH	4Kword PARAMETER BLOCK
04000H-05FFFH	02000H-02FFFH	4Kword PARAMETER BLOCK
00000H-03FFFH	00000H-01FFFH	8Kword BOOT BLOCK

A₁₋₁-A₁₈(Byte mode) A₀-A₁₈(Word mode)

M5M29FB800 Memory Map

x8 (Byte mode) x16 (Word mode)		
FC000H-FFFFFH	7E000H-7FFFFH	8Kword BOOT BLOCK
FA000H-FBFFFFH	7D000H-7DFFFFH	4Kword PARAMETER BLOCK
F8000H-F9FFFFH	7C000H-7CFFFFH	4Kword PARAMETER BLOCK
F0000H-F7FFFFH	78000H-7BFFFFH	16Kword MAIN BLOCK
E0000H-EFFFFH	70000H-77FFFH	32Kword MAIN BLOCK
D0000H-DFFFFH	68000H-6FFFFH	32Kword MAIN BLOCK
C0000H-CFFFFH	60000H-67FFFH	32Kword MAIN BLOCK
B0000H-BFFFFH	58000H-5FFFFH	32Kword MAIN BLOCK
A0000H-AFFFFH	50000H-57FFFH	32Kword MAIN BLOCK
90000H-9FFFFH	48000H-4FFFFH	32Kword MAIN BLOCK
80000H-8FFFFH	40000H-47FFFH	32Kword MAIN BLOCK
70000H-7FFFFH	38000H-3FFFFH	32Kword MAIN BLOCK
60000H-6FFFFH	30000H-37FFFH	32Kword MAIN BLOCK
50000H-5FFFFH	28000H-2FFFFH	32Kword MAIN BLOCK
40000H-4FFFFH	20000H-27FFFH	32Kword MAIN BLOCK
30000H-3FFFFH	18000H-1FFFFH	32Kword MAIN BLOCK
20000H-2FFFFH	10000H-17FFFH	32Kword MAIN BLOCK
10000H-1FFFFH	08000H-0FFFFH	32Kword MAIN BLOCK
00000H-0FFFFH	00000H-07FFFH	32Kword MAIN BLOCK

A₁₋₁-A₁₈(Byte mode) A₀-A₁₈(Word mode)

M5M29FT800 Memory Map

BUS OPERATIONS

Bus Operations for Word-Wide Mode (/BYTE=VIH)

Mode		Pins	/CE	/OE	/WE	/RP	DQ ₀₋₁₅	RY/ $\overline{\text{BY}}$
Read	Array		V _{IL}	V _{IL}	V _{IH}	V _{IH}	Data out	V _{OH} (Hi-Z)
	Status Register		V _{IL}	V _{IL}	V _{IH}	V _{IH}	Status Register Data	X ¹⁾
	Lock Bit Status		V _{IL}	V _{IL}	V _{IH}	V _{IH}	Lock Bit Data (DQ ₆)	X
	Identifier Code		V _{IL}	V _{IL}	V _{IH}	V _{IH}	Identifier Code	V _{OH} (Hi-Z)
Output disable			V _{IL}	V _{IH}	V _{IH}	V _{IH}	Hi-Z	X
Stand by			V _{IH}	X ²⁾	X	V _{IH}	Hi-Z	X
Write	Program		V _{IL}	V _{IH}	V _{IL}	V _{IH}	Command/Data in	X
	Erase		V _{IL}	V _{IH}	V _{IL}	V _{IH}	Command	X
	Others		V _{IL}	V _{IH}	V _{IL}	V _{IH}	Command	X
Deep Power Down			X	X	X	V _{IL}	Hi-Z	V _{OH} (Hi-Z)

Bus Operations for Byte-Wide Mode (BYTE=VIL)

Mode		Pins	/CE	/OE	/WE	/RP	DQ ₀₋₇	RY/ $\overline{\text{BY}}$
Read	Array		V _{IL}	V _{IL}	V _{IH}	V _{IH}	Data out	V _{OH} (Hi-Z)
	Status Register		V _{IL}	V _{IL}	V _{IH}	V _{IH}	Status Register Data	X ¹⁾
	Lock Bit Status		V _{IL}	V _{IL}	V _{IH}	V _{IH}	Lock Bit Data (DQ ₆)	X
	Identifier Code		V _{IL}	V _{IL}	V _{IH}	V _{IH}	Identifier Code	V _{OH} (Hi-Z)
Output disable			V _{IL}	V _{IH}	V _{IH}	V _{IH}	Hi-Z	X
Stand by			V _{IH}	X ²⁾	X	V _{IH}	Hi-Z	X
Write	Program		V _{IL}	V _{IH}	V _{IL}	V _{IH}	Command/Data in	X
	Erase		V _{IL}	V _{IH}	V _{IL}	V _{IH}	Command	X
	Others		V _{IL}	V _{IH}	V _{IL}	V _{IH}	Command	X
Deep Power Down			X	X	X	V _{IL}	Hi-Z	V _{OH} (Hi-Z)

1) X at RY/ $\overline{\text{BY}}$ is VOL or VOH(Hi-Z).

*The RY/ $\overline{\text{BY}}$ is an open drain output pin and indicates status of the internal WSM. When low, it indicates that the WSM is Busy performing an operation. A pull-up resistor of 10K-100K Ohms is required to allow the RY/ $\overline{\text{BY}}$ signal to transition high indicating a Ready WSM condition.

2) X can be VIH or VIL for control pins.

M5M29FB/T800FP, VP, RV-80,-10,-12

8,388,608-BIT (1048,576-WORD BY 8-BIT / 524,288-WORD BY16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

SOFTWARE COMMAND DEFINITION

Command List

Command	1st bus cycle			2nd bus cycle			3rd bus cycle		
	Mode	Address	Data (D7-0)	Mode	Address	Data (D7-0)	Mode	Address	Data (D7-0)
Read Array	Write	X	FFH						
Device Identifier	Write	X	90H	Read	IA ²⁾	ID ²⁾			
Read Status Register	Write	X	70H	Read	X	SRD ³⁾			
Clear Status Register	Write	X	50H						
Page Program ⁴⁾	Write	X	41H	Write	WA0 ⁴⁾	WD0 ⁴⁾	Write	WA1	WD1
Block Erase / Confirm	Write	X	20H	Write	BA ⁵⁾	D0H			
Suspend	Write	X	B0H						
Resume	Write	X	D0H						
Read Lock Bit Status	Write	X	71H	Read	BA	DQ6 ⁶⁾			
Lock Bit Program / Confirm	Write	X	77H	Write	BA	D0H			
Erase All Unlocked Blocks	Write	X	A7H	Write	X	D0H			
Sleep ⁷⁾	Write	X	F0H						

- 1) In the word-wide mode, upper byte data (D8-D15) is ignored.
- 2) IA=ID Code Address : A0=VIL (Manufacturer's Code) : A0=VIH (Device Code), ID=ID Code, /BYTE =VIL : A-1, A1-A18 = VIL, /BYTE =VIH : A1-A18 = VIL
- 3) SRD = Status Register Data
- 4) WA=Write Address, WD=Write Data.
/BYTE =VIL : Write Address and Write Data must be provided sequentially from 00H to FFH for A-1-A6. Page size is 256Byte (256byte x 8bit), /BYTE =VIH : Write Address and Write Data must be provided sequentially from 00H to 7FH for A0-A6. Page size is 128word (128word x 16bit).
- 5) BA = Block Address (Addresses except Block Address must be VIH.)
- 6) DQ6 provides Block Lock Status, DQ6 = 1 : Block Unlock, DQ6 = 0 : Block Locked.
- 7) Sleep command (F0H) put the device into the sleep mode after completing the current operation. The active current is reduced to deep power -down levels. The Read Array command (FFH) must be written to get the device out of sleep mode.

BLOCK LOCKING

SOP Package		TSOP Package			Write Protection Provided
/RP	Lock Bit(Internally)	/RP	/WP	Lock Bit(Internally)	
VIL	X	VIL	X	X	All Blocks Locked (Deep Power Down Mode)
VHH	X	VHH	X	X	All Blocks UnLocked
VIH	0	VIH	VIL	0	Blocks Locked (Depend on Lock Bit Data)
VIH	1	VIH	VIL	1	Blocks Unlocked (Depend on Lock Bit Data)
		VIH	VIH	X	All Blocks Unlocked

D6 provides Lock Status of each block after writing the Read Lock Status command (71H).
In case of TSOP package, /WP pin must not be switched during performing Read / Write operations or WSM Busy (WSMS = 0).

STATUS REGISTER

Symbol	Status	Definition	
		"1"	"0"
SR.7 (D7)	Write State Machine Status	Ready	Busy
SR.6 (D6)	Suspend Status	Suspended	Operation in Progress / Completed
SR.5 (D5)	Erase Status	Error	Successful
SR.4 (D4)	Program Status	Error	Successful
SR.3 (D3)	Block Status after Program	Error	Successful
SR.2 (D2)	<i>Reserved</i>	-	-
SR.1 (D1)	<i>Reserved</i>	-	-
SR.0 (D0)	Device Sleep Status	Device in Sleep	Device Not in Sleep

*The RY/BY is an open drain output pin and indicates status of the internal WSM. When low, it indicates that the WSM is Busy performing an operation. A pull-up resistor of 10K-100K Ohms is required to allow the RY/BY signal to transition high indicating a Ready WSM condition.

*D3 indicates the block status after the page programming. When D3 is "1", the page has the over-programmed cell. If over-program occurs, the device is block fail. However if D3 is "1", please try the block erase to the block. The block may revive.

DEVICE IDENTIFIER CODE

Code	Pins	A0	D7	D6	D5	D4	D3	D2	D1	D0	Hex. Data
		Manufacturer Code	VIL	0	0	0	1	1	1	0	0
Device Code (-T)	VIH	0	1	0	1	1	1	0	1	5DH	
Device Code (-B)	VIH	0	1	0	1	1	1	1	0	5EH	

In the word-wide mode, the same data as D7-0 is read out from D15-8.
A9 = VHH Mode : A9 = 11.5V~13.0V. Set A9 to VHH min.200ns before falling edge of /CE in ready status. Min.200ns after return to VIH, device can't be accessed.
A1~A8, A10~A18, /CE, /OE = VIL, /WE = VIH
D15/A-1 = VIL (/BYTE = L)

M5M29FB/T800FP, VP, RV-80,-10,-12
8,388,608-BIT (1048,576-WORD BY 8-BIT / 524,288-WORD BY16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	V _{CC} voltage	With respect to Ground	-0.2	4.6	V
V _{I1}	All input or output voltage except V _{CC} ,A ₉ /RP ¹⁾		-0.6	4.6	V
V _{I2}	A ₉ ,RP supply voltage		-0.6	14.0	V
T _a	Ambient temperature		0	70	°C
T _{bs}	Temperature under bias		-10	80	°C
T _{stg}	Storage temperature		-65	125	°C
I _{OUT}	Output short circuit current			100	mA

1) Minimum DC voltage is -0.5V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins is V_{CC}+0.5V which, during transitions, may overshoot to V_{CC}+1.5V for periods <20ns.

CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _{IN}	Input capacitance (Address, Control Pins)	T _a = 25°C, f = 1MHz, V _{in} = V _{out} = 0V			8	pF
C _{OUT}	Output capacitance				12	pF

DC ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 3.3V±0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ ¹⁾	Max	
I _{LI}	Input leakage current	0V V _{IN} V _{CC}			±1.0	µA
I _{LO}	Output leakage current	0V V _{OUT} V _{CC}			±10	µA
ISB1	V _{CC} standby current	V _{CC} = 3.6V, V _{IN} =V _{IL} /V _{IH} , /CE = /RP =/WP = V _{IH}		50	200	µA
ISB2		V _{CC} = 3.6V, V _{IN} =GND or V _{CC} , /CE = /RP = /WP= V _{CC} ±0.3V		1	5	µA
ISB3		V _{CC} = 3.6V, V _{IN} =V _{IL} /V _{IH} , /RP = V _{IL}		5	15	µA
ISB4	V _{CC} deep powerdown current	V _{CC} = 3.6V, V _{IN} =GND or V _{CC} , /RP =GND±0.3V		1	5	µA
I _{CC1}	V _{CC} read current for Word or Byte	V _{CC} = 3.6V, V _{IN} =V _{IL} /V _{IH} , /CE = V _{IL} , /RP=OE=V _{IH} , f = 10MHz, I _{OUT} = 0mA		7	25	mA
I _{CC2}	V _{CC} Write current for Word or Byte	V _{CC} = 3.6V, V _{IN} =V _{IL} /V _{IH} , /CE =/WE= V _{IL} , /RP=/OE=V _{IH}			30	mA
I _{CC3}	V _{CC} program current	V _{CC} = 3.6V, V _{IN} =V _{IL} /V _{IH} , /CE = /RP =/WP = V _{IH}			40	mA
I _{CC4}	V _{CC} erase current	V _{CC} = 3.6V, V _{IN} =V _{IL} /V _{IH} , /CE = /RP =/WP = V _{IH}			40	mA
I _{CC5}	V _{CC} suspend current	V _{CC} = 3.6V, V _{IN} =V _{IL} /V _{IH} , /CE = /RP =/WP = V _{IH}			200	µA
I _{RP}	/RP all block unlock current	/RP = V _{IH} max			100	µA
I _{ID}	A ₉ intelligent identifier current	A ₉ = V _{ID} max			100	µA
V _{IHH}	/RP unlock voltage		11.4	12.0	12.6	V
V _{ID}	A ₉ intelligent identifier voltage		11.4	12.0	12.6	V
V _{IL}	Input low voltage		-0.5		0.8	V
V _{IH}	Input high voltage		2.0		V _{CC} +0.5	V
V _{OL}	Output low voltage	I _{OL} = 5.8mA			0.45	V
V _{OH1}	Output high voltage	I _{OH} = -2.5mA	0.85V _{CC}			V
V _{OH2}		I _{OH} = -100µA	V _{CC} -0.4			V
V _{LKO}	Low V _{CC} Lock-Out voltage 2)		1.5		2.5	V

All currents are in RMS unless otherwise noted.

1) Typical values at V_{CC}=3.3V, T_a=25°C

2) To protect against initiation of write cycle during V_{CC} power-up/ down, a write cycle is locked out for V_{CC} less than V_{LKO}.

If V_{CC} is less than V_{LKO}, Write State Machine is reset to read mode. When the Write State Machine is in Busy state, if V_{CC} is less than V_{LKO}, the alteration of memory contents may occur.

M5M29FB/T800FP, VP, RV-80, -10, -12
8,388,608-BIT (1048,576-WORD BY 8-BIT / 524,288-WORD BY16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

AC ELECTRICAL CHARACTERISTICS (Ta = 0 ~70°C, Vcc = 3.3±0.3V)

Read-Only Mode

Symbol		Parameter	Limits									Unit
			M5M29FB/T800-80			M5M29FB/T800-10			M5M29FB/T800-12			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
tRC	tAVAV	Read cycle time	80			100			120			ns
ta (AD)	tAVQV	Address access time			80			100			120	ns
ta (CE)	tELQV	Chip enable access time			80			100			120	ns
ta (OE)	tGLQV	Output enable access time			40			50			60	ns
tCLZ	tELQX	Chip enable to output in low-Z	0			0			0			ns
tDF(CE)	tEHQZ	Chip enable high to output in high Z			25			25			30	ns
tOLZ	tGLQX	Output enable to output in low-Z	0			0			0			ns
tDF(OE)	tGHQZ	Output enable high to output in high Z			25			25			30	ns
tPHZ	tPLQZ	/RP low to output high-Z			150			150			300	ns
ta(BYTE)	tFL/HQV	/BYTE access time			80			100			120	ns
tBHZ	tFLQZ	/BYTE low to output high-Z			25			25			30	ns
tOH	tOH	Output hold from /CE, /OE, addresses	0			0			0			ns
tBCD	tELFL/H	/CE low to /BYTE high or low			5			5			5	ns
tBAD	tAVFL/H	Address to /BYTE high or low			5			5			5	ns
tOEH	tWHGL	/OE hold from /WE high	80			100			120			ns
tPS	tPHL	/RP recovery to /CE low	500			500			500			ns

Timing measurements are made under AC waveforms for read operations.

AC ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, Vcc = 3.3V±0.3V)

Write Mode (/WE control)

Symbol		Parameter	Limits									Unit
			M5M29FB/T800-80			M5M29FB/T800-10			M5M29FB/T800-12			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
tWC	tAVAV	Write cycle time	80			100			120			ns
tAS	tAVWH	Address set-up time	50			50			50			ns
tAH	tWHAX	Address hold time	10			10			10			ns
tDS	tDVWH	Data set-up time	50			50			50			ns
tDH	tWHDX	Data hold time	10			10			10			ns
tCS	tELWL	Chip enable set-up time	0			0			0			ns
tCH	tWHEH	Chip enable hold time	0			0			0			ns
tWP	tWLWH	Write pulse width	60			60			60			ns
tWPH	tWHWL	Write pulse width high	20			20			20			ns
tBS	tFL/HWH	Byte enable high or low set-up time	50			50			50			ns
tBH	tWHFL/H	Byte enable high or low hold time	80			100			120			ns
tBLS	tPHHWH	Block Lock set-up to write enable high	80			100			120			ns
tWPS												
tBLH	tQVPH	Block Lockhold from valid SRD	0			0			0			ns
tWPH												
tDAP	tWHRH1	Duration of auto-program operation		7.5	120		7.5	120		7.5	120	ms
tDAE	tWHRH2	Duration of auto-block erase operation		50	600		50	600		50	600	ms
tWHRL	tWHRL	Write enable high to RY/ $\overline{\text{BY}}$ low			80			100			120	ns
tPS	tPHWL	/RP high recovery to write enable low	500			500			500			ns

Read timing parameters during command write operations mode are the same as during read-only operations mode.
 Typical values at Vcc=3.3V, Ta=25°C

M5M29FB/T800FP, VP, RV-80, -10, -12

8,388,608-BIT (1048,576-WORD BY 8-BIT / 524,288-WORD BY16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

AC ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, Vcc = 3.3V±0.3V)

Write Mode (/CE control)

Symbol		Parameter	Limits									Unit
			M5M29FB/T800-80			M5M29FB/T800-10			M5M29FB/T800-12			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
tWC	tAVAV	Write cycle time	80			100			120			ns
tAS	tAVEH	Address set-up time	50			50			50			ns
tAH	tEHAX	Address hold time	10			10			10			ns
tDS	tDVEH	Data set-up time	50			50			50			ns
tDH	tEHDX	Data hold time	10			10			10			ns
tWS	tWLEL	Write enable set-up time	0			0			0			ns
tWH	tEHWL	Write enable hold time	0			0			0			ns
tCEP	tELEH	/CE pulse width	60			60			60			ns
tCEPH	tEHEL	/CE pulse width high	20			20			20			ns
tBS	tFL/HEH	Byte enable high or low set-up time	50			50			50			ns
tBH	tEHL/H	Byte enable high or low hold time	80			100			120			ns
tBLS	tPHHEH	Block Lock set-up to write enable high	80			100			120			ns
tWPS												
tBLH	tQVPH	Block Lockhold from valid SRD	0			0			0			ns
tWPH												
tDAP	tEHRH1	Duration of auto-program operation		7.5	120		7.5	120		7.5	120	ms
tDAE	tEHRH2	Duration of auto-block erase operation		50	600		50	600		50	600	ms
tEHL	tEHL	/CE enable high to RY/ \overline{BY} low			80			100			120	ns
tPS	tPEL	/RP high recovery to write enable low	500			500			500			ns

Read timing parameters during command write operations mode are the same as during read-only operations mode.
Typical values at Vcc=3.3V, Ta=25°C

Erase and Program Performance

Parameter	Min	Typ	Max	Unit
Block Erase Time		50	600	ms
Main Block Write Time (Page Mode)		1.9	3.8	sec
Page Write Time		7.5	120	ms

Vcc Power Up / Down Timing

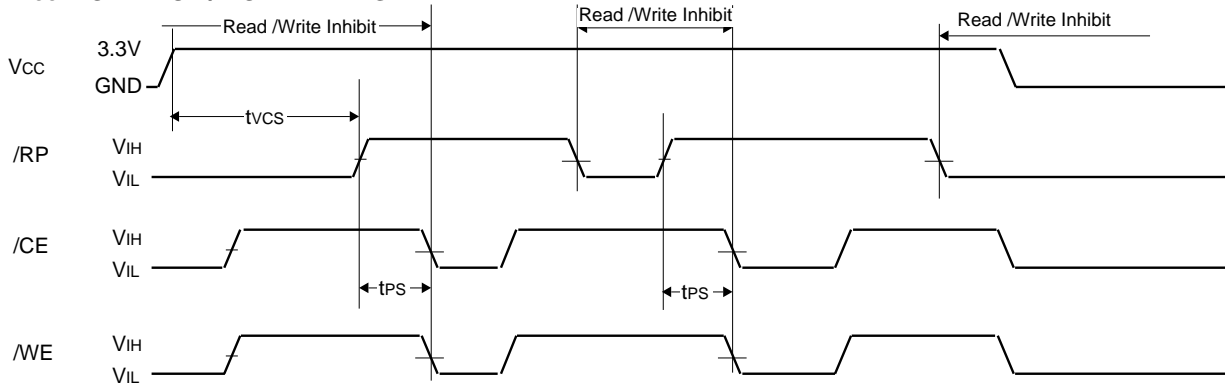
Symbol	Parameter	Min	Typ	Max	Unit
tVCS	/RP =VIH set-up time from Vccmin	2			μs

During power up/down, by the noise pulses on control pins, the device has possibility of accidental erasure or programming.
The device must be protected against initiation of write cycle for memory contents during power up/down.
The delay time of min.2μsec is always required before read operation or write operation is initiated from the time Vcc reaches Vccmin during power up/down. By holding /RP VIL, the contents of memory is protected during Vcc power up/down.
During power up, /RP must be held VIL for min.2μs from the time Vcc reaches Vccmin.
During power down, /RP must be held VIL until Vcc reaches GND.
/RP doesn't have latch mode, so /RP must be held VIH during read operation or erase/program operation.

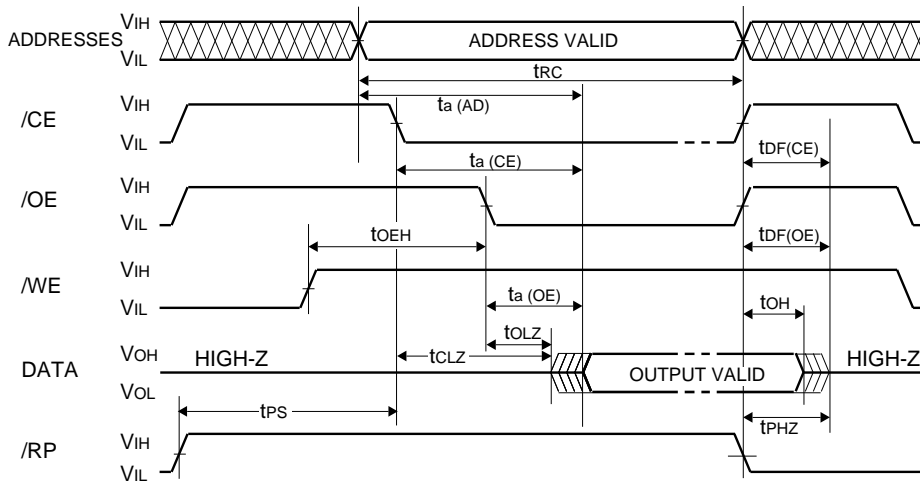
M5M29FB/T800FP, VP, RV-80, -10, -12

8,388,608-BIT (1048,576-WORD BY 8-BIT / 524,288-WORD BY16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

V_{CC} POWER UP / DOWN TIMING



AC WAVEFORMS FOR READ OPERATION AND TEST CONDITIONS



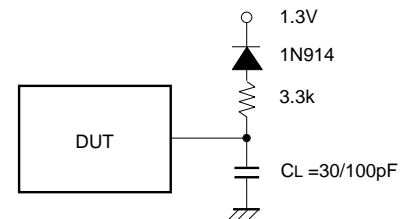
TEST CONDITIONS FOR AC CHARACTERISTICS

Input voltage : $V_{IL} = 0V$, $V_{IH} = 3.0V$
Input rise and fall times : 5ns (80ns)
10ns (100/120ns)

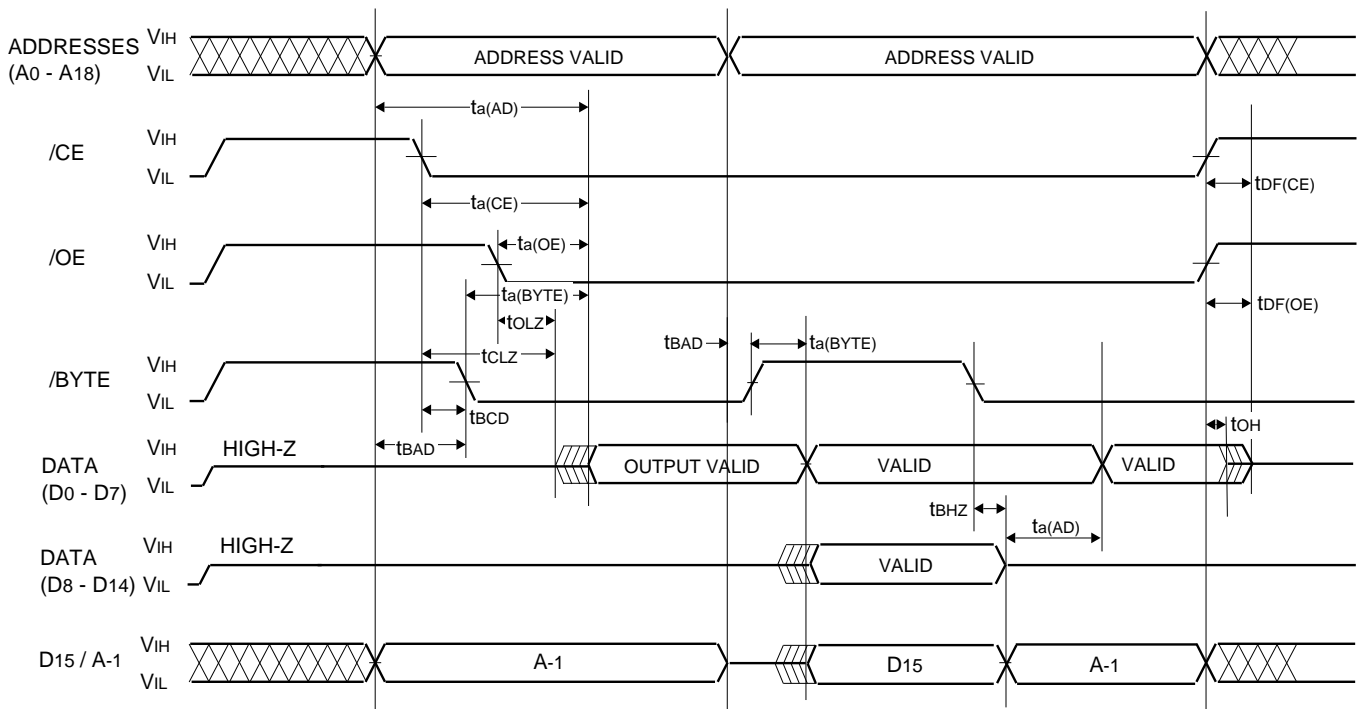
Reference voltage at timing measurement : 1.5V

Output load : 1TTL gate +
CL(100pF for 100/120ns)
CL(30pF for 80ns)

or



BYTE AC WAVEFORMS FOR READ OPERATION

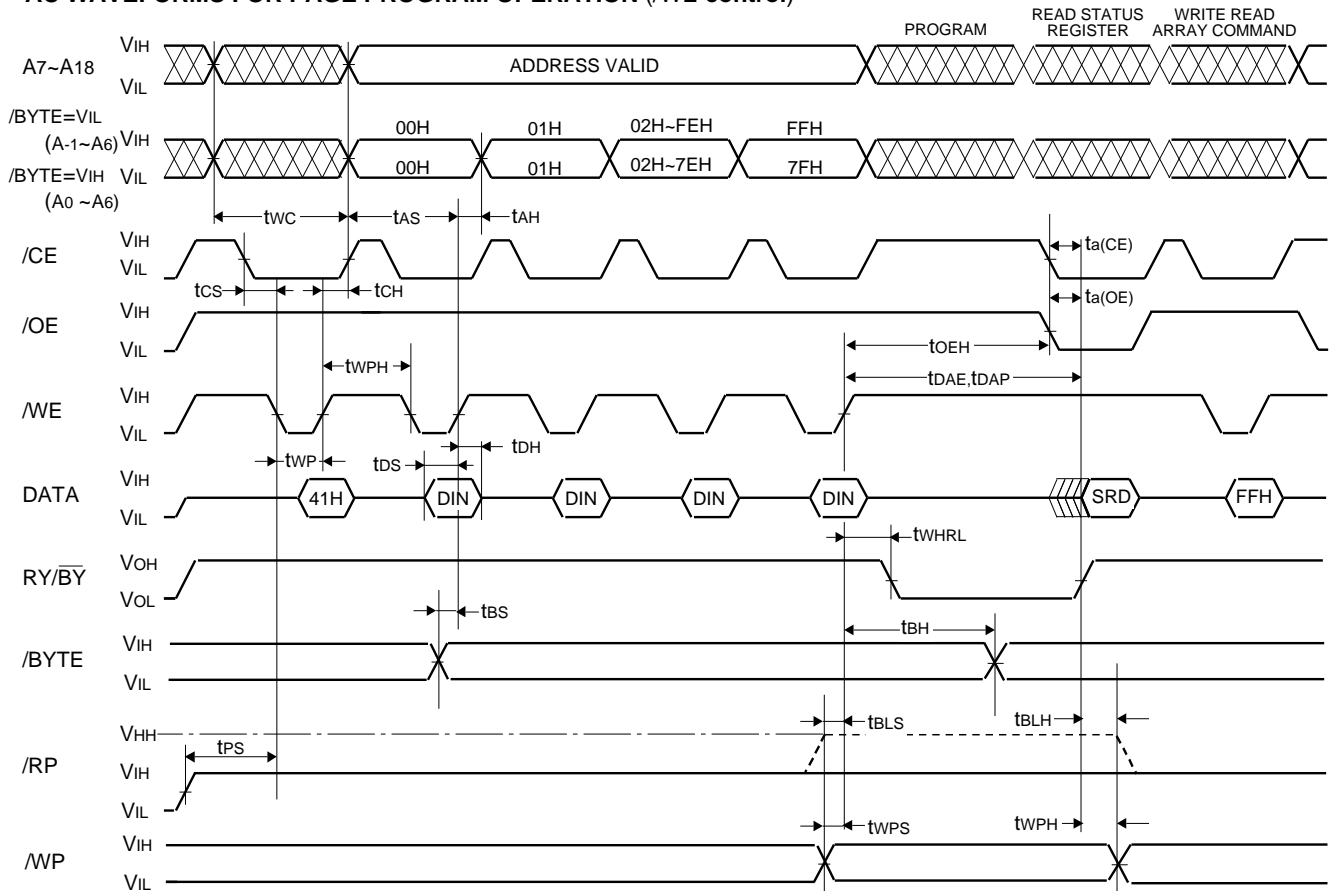


When /BYTE= V_{IH} , /CE=/OE= V_{IL} , D15/A-1 is output status. At this time, input signal must not be applied.

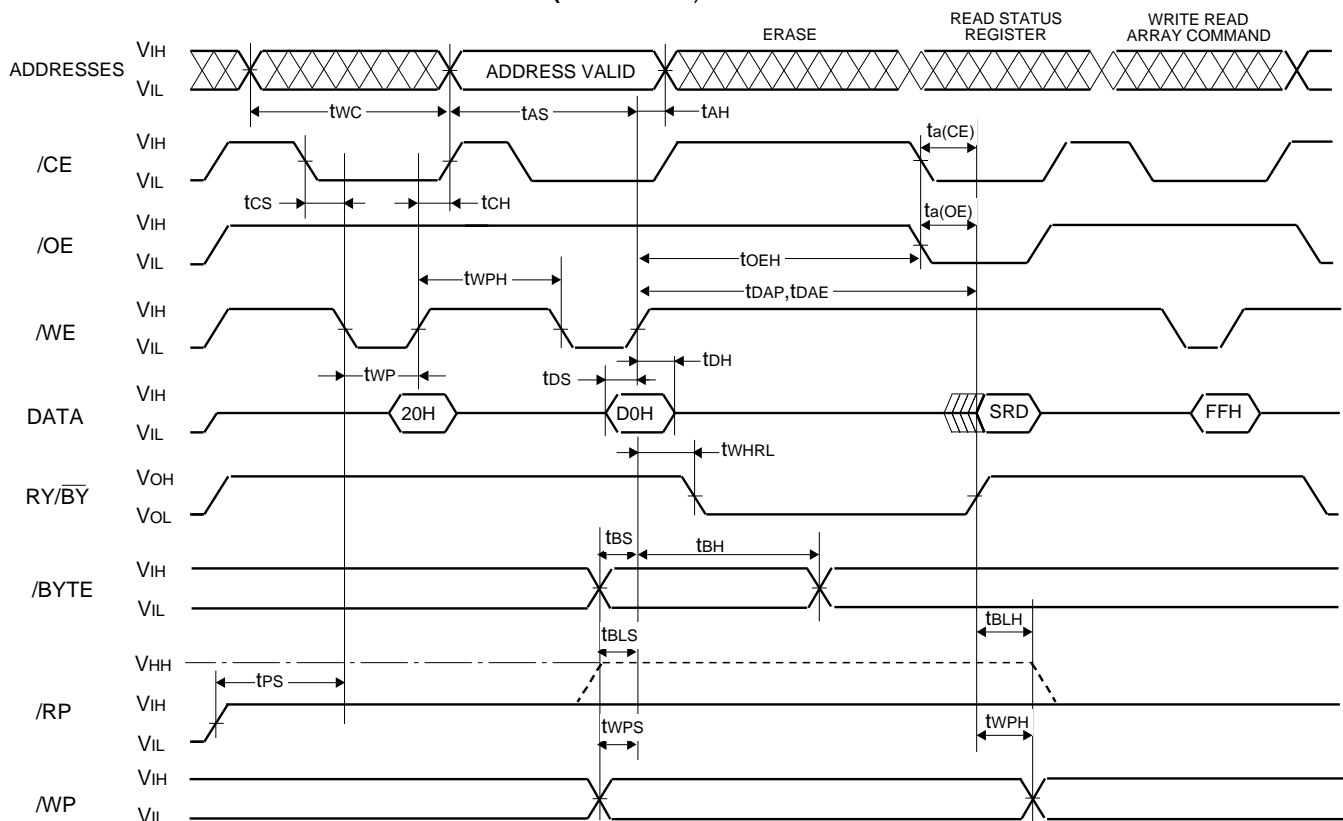
M5M29FB/T800FP, VP, RV-80, -10, -12

8,388,608-BIT (1048,576-WORD BY 8-BIT / 524,288-WORD BY16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

AC WAVEFORMS FOR PAGE PROGRAM OPERATION (/WE control)



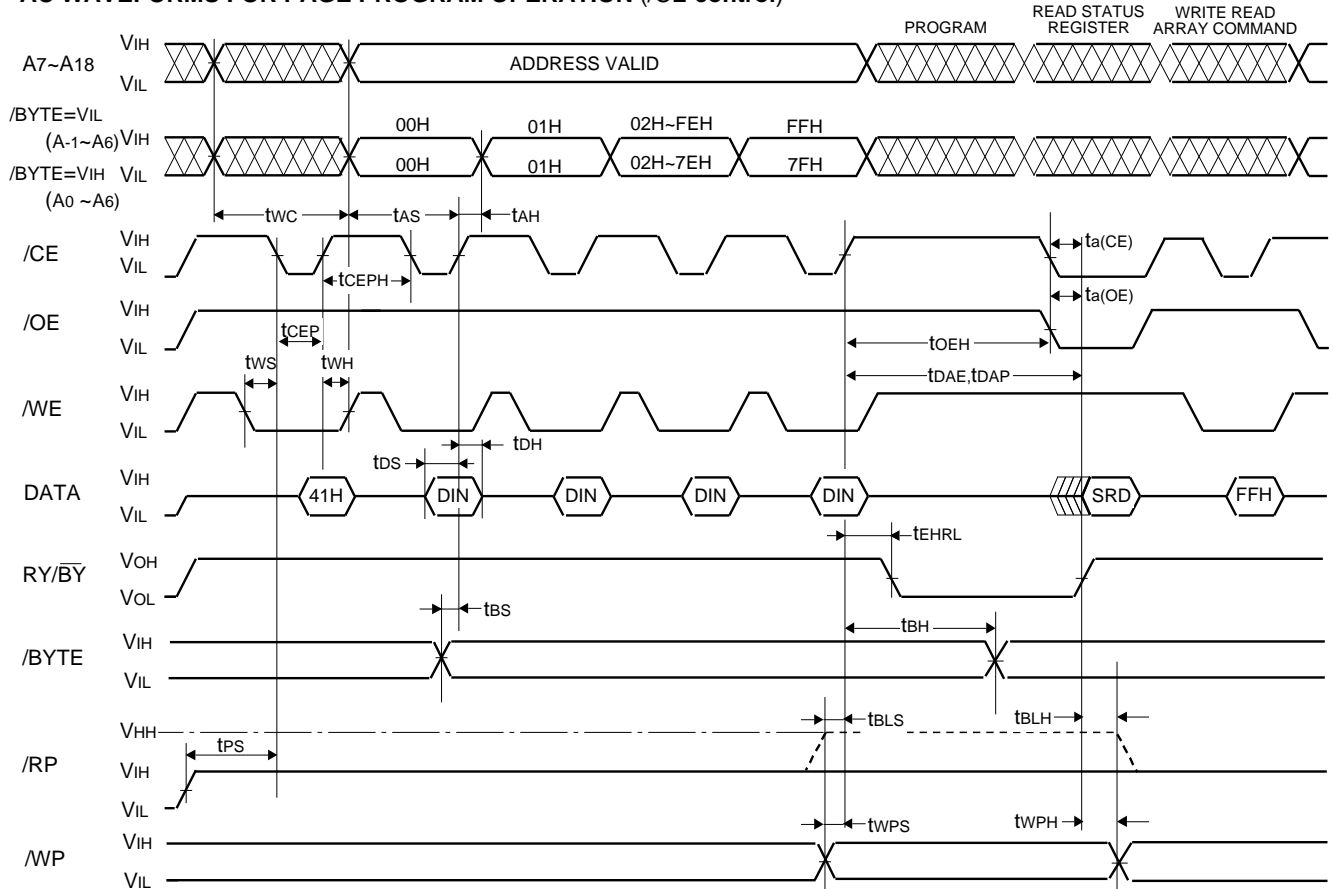
AC WAVEFORMS FOR ERASE OPERATIONS (/WE control)



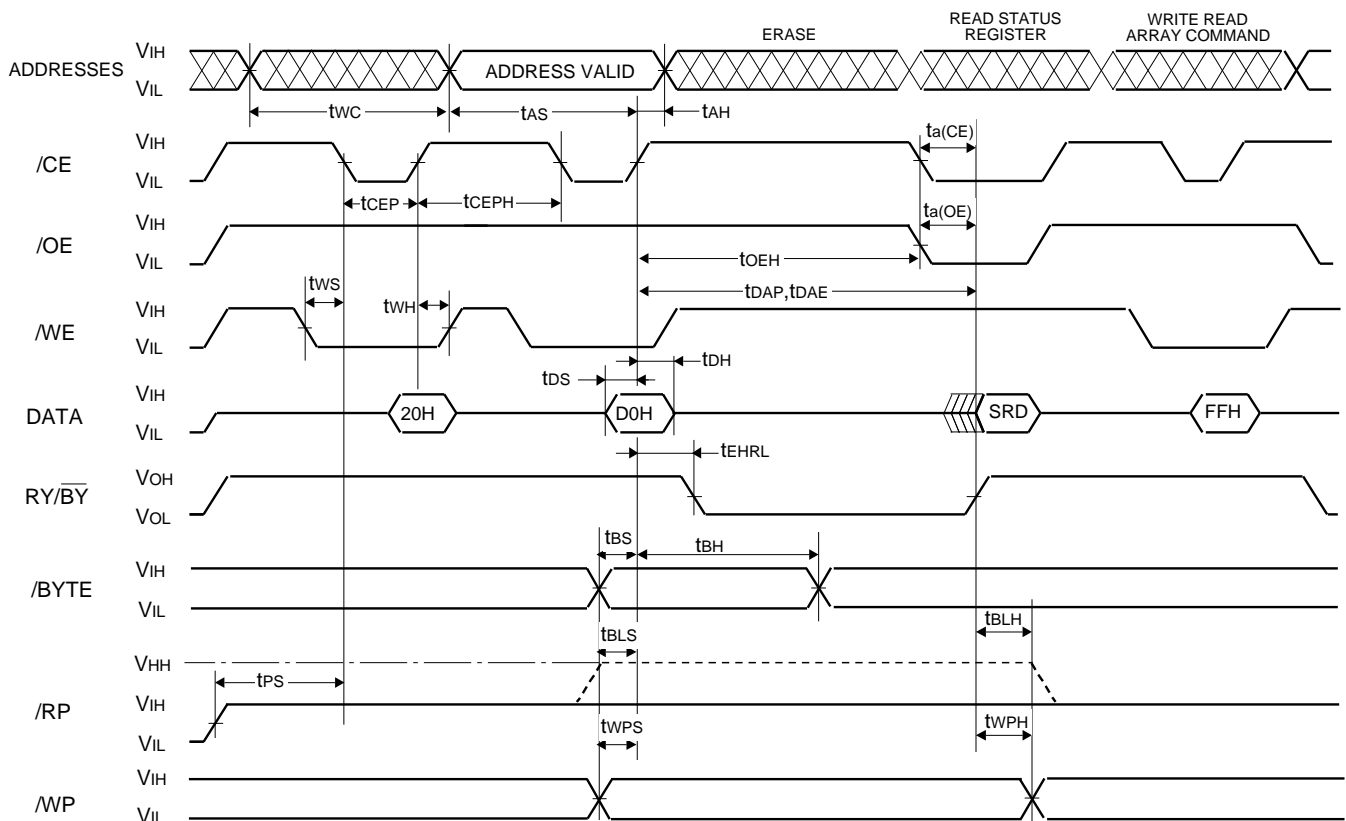
M5M29FB/T800FP, VP, RV-80, -10, -12

8,388,608-BIT (1048,576-WORD BY 8-BIT / 524,288-WORD BY 16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

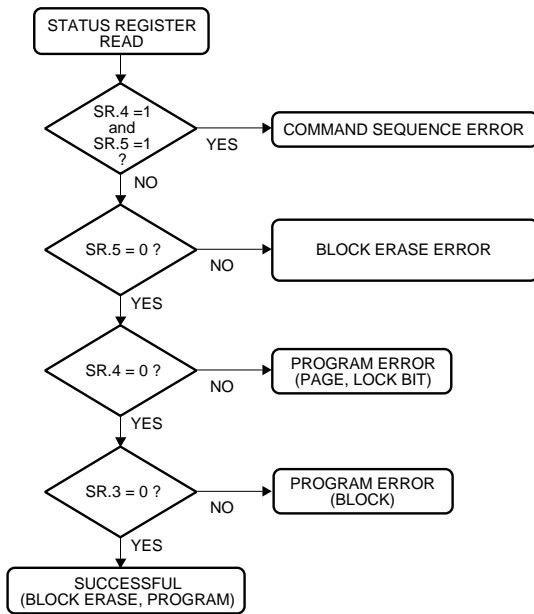
AC WAVEFORMS FOR PAGE PROGRAM OPERATION (/CE control)



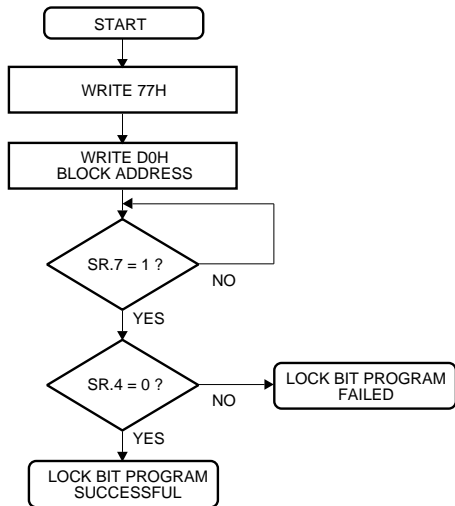
AC WAVEFORMS FOR ERASE OPERATIONS (/CE control)



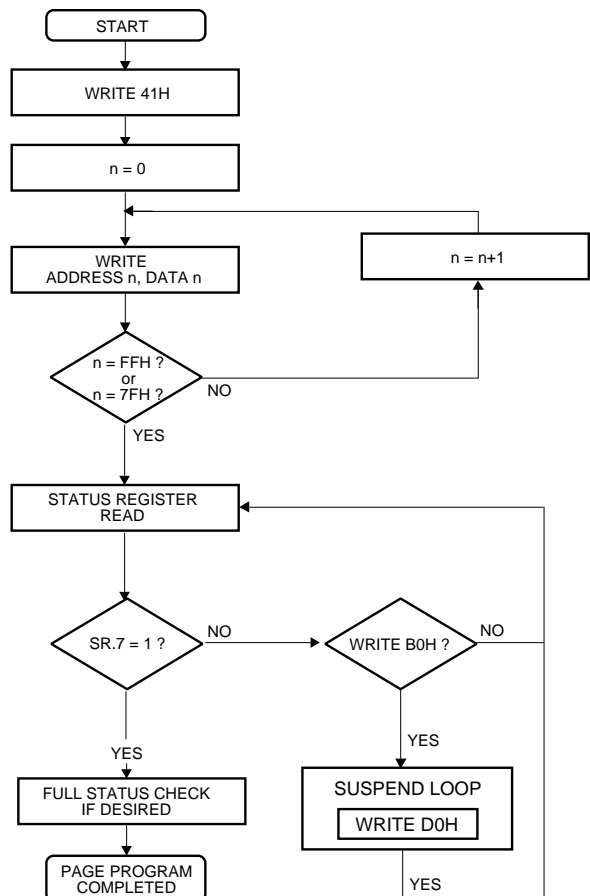
FULL STATUS CHECK PROCEDURE



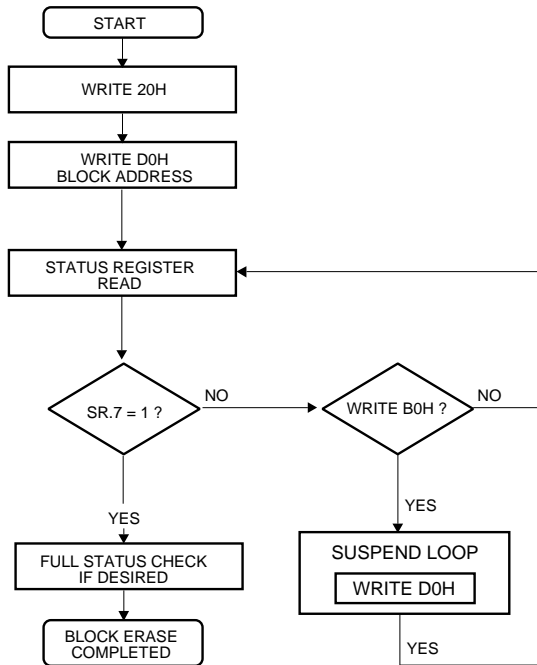
LOCK BIT PROGRAM FLOW CHART



PAGE PROGRAM FLOW CHART



BLOCK ERASE FLOW CHART



SUSPEND / RESUME FLOW CHART

